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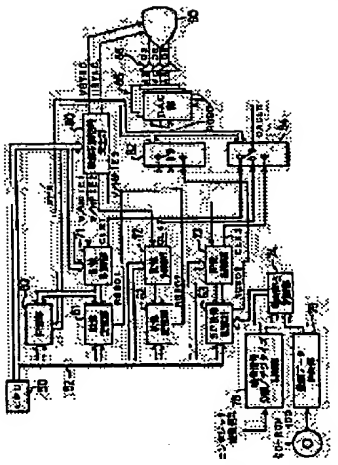
(54) VIDEO DISPLAY DEVICE

(57)Abstract:

PURPOSE: To display plural videos on one screen while superposing them according to video data stored in respective video memories without transferring video data among plural memories.

CONSTITUTION: Three storage control parts 71 to 73 output clock signals CLK1 to CLK3 synchronizing with three video signals RGB01 to 03 readout respectively from three video storage parts 61 to 63. A video signal switching part 82 selects one of three video signals and a clock signal switching part 84 selects one of three clock signals. A D/A converting part 86 D/A-converts the selected video signal with the selected clock signal. A video control signal generating part 80 switches respective video signals in one screen by supplying read-out permission signals HPIE1 to 3, VPIE1 to 3 to three storage control parts 71 to 73 respectively. Thus, videos expressed by video signals readout from three video storage parts 61 to 63 are displayed on one screen while being superposed.



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CLAIMS

[Claim(s)]
[Claim 1] Two or more image memory which is the graphic display devices which display two or more images on the one display screen in piles, and memorizes two or more video signals, respectively, An image control signal generating means to generate two or more read-out enabling signals which show the timing which reads two or more video signals from said two or more image memory, respectively, While giving two or more read-out control signals for reading said two or more video signals to said two or more image memory, respectively, corresponding respectively to said two or more read-out enabling signals The memory control means which generates two or more clock signals which synchronize with said two or more video signals read from said two or more image memory, respectively, A selection-signal generation means to generate the image selection signal for choosing switching one of said two or more of the video signals in two or more predetermined locations in the screen of said display, A graphic display device equipped with a display means to display an image according to a selection means to choose one of said two or more of the video signals, and one of said two or more of the clock signals according to the image selection signal given from said selection-signal generation section, and the video signal and clock signal which were chosen with said selection means.
[Claim 2] It is a graphic display device according to claim 1. Said selection-signal generation means It has the memory area of the predetermined number of bits which two or more pixels contained in a field predetermined [on the screen of said display means] are alike, respectively, and corresponds. The memory which memorizes the image select data showing any of two or more of said video signals are chosen about each of two or more of said pixels, A graphic display device including a control signal supply means to supply the select data read-out control signal for reading said image select data from said memory as said image selection signal to said memory.
[Claim 3] It is the graphic display device which is the transfer way which it is a graphic display device according to claim 2, and said control signal supply means makes one of said two or more read-out control signals said select data read-out control signal, and is transmitted to said memory.
[Claim 4] It is a graphic display device containing the D-A converter which is a graphic display device according to claim 1, and changes into an analog video signal the digital video signal chosen with said selection means according to the clock signal as which said display means was chosen with said selection means.
[Claim 5] It is a graphic display device according to claim 1. Said image control signal generating means A means to generate the 1st signal which has the 1st period equivalent to the scan period of the one scanning line on the screen of said display means is included. Said memory control means It is based on said 1st signal given from said image control signal generating means, and is N1 of said 1st period. The 1st PLL circuit which generates the 1st clock signal which has a twice (N1 is an integer) as many period as this, A level address-generation means to generate the level address of the 1st image memory which is one of said two or more of the image memory, By adding a perpendicular address-generation means to generate the perpendicular address of said 1st image memory, and said level address and said perpendicular address Said level address-generation means is a graphic display device including the renewal means of the level address to which said level address is made to increase according to the

pulse of said 1st clock signal while the adder which generates the address given to said 1st image memory is included.
[Claim 6] While being a graphic display device according to claim 6 and connecting the processor in which arithmetic logical operation is still more possible, said processor, and said two or more image memory It has the bus which connects said processor and said memory control section. Said processor Said integer N1 in said 1st PLL circuit Graphic display device which carries out variable power of the 1st image displayed on said display means by the 1st video signal read from said 1st image memory by changing a value horizontally.
[Claim 7] It is a graphic display device according to claim 6. Said image control signal generating means A means to generate the 2nd signal which has the 2nd period equivalent to the scan period for one screen of said display means is included. Said 1st memory control means Furthermore, it is based on said 1st signal given from said image control signal generating means. A means to generate the 1st renewal signal of the scanning line which shows the timing equivalent to the termination of the scanning line about the 1st video signal read from said 1st image memory, Based on either of said 1st and 2nd signals, the 2nd PLL circuit which generates the 2nd renewal signal of the scanning line which has a period twice (N2 is an integer) the N of said 2nd period is included. Said level address-generation means includes a means to reset said level address to predetermined initial value according to one pulse of said 1st renewal signal of the scanning line. Said perpendicular address-generation means Said pulse number of the 2nd renewal signal of the scanning line given according to one pulse of said 1st renewal signal of the scanning line between the two newest pulses of said 1st renewal signal of the scanning line, A graphic display device including a renewal means of the perpendicular address to update said perpendicular address by adding the perpendicular address increment equivalent to the result of having carried out the multiplication of the difference of the address equivalent to a predetermined number in said display means of scanning lines to said perpendicular address.
[Claim 8] It is said integer [in / it is a graphic display device according to claim 7, and / in said processor / said 2nd PLL circuit] N2. Graphic display device which carries out variable power of the 1st image displayed on said display means by the 1st video signal read from said 1st image memory by changing a value perpendicularly.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the graphic display device which displays two or more images on the same screen based on the video signal memorized by two or more image memory.
[0002]
[Description of the Prior Art] Drawing 34 is the explanatory view showing the display action of the image in the conventional graphic display device. In a personal computer in recent years, two or more OS's

(operating system) may work. Drawing 34 (A) shows the condition of having displayed the screen by MS-DOS (trademark of Microsoft Corp.) which is the 2nd OS into the window of MS-WINDOWS (trademark of Microsoft Corp.) which is the 1st OS. Drawing 34 (B) and (C) show the address space of two OS's in this case.

[0003]

[Problem(s) to be Solved by the Invention] In order to display the screen of the 2nd OS on one of the windows by the 1st OS conventionally, as drawing 34 (B) showed and an arrow head showed to (C), image data needed to be transmitted to the video memory (AVRAM) for a display in the 1st OS from the video memory (VRAM) for a display in the 2nd OS. Since CPU performed the image data transfer, it will be used for the processing most processing times of whose of CPU display the screen by the 2nd OS, and there was a problem that other processings by CPU will become very slow. Such a problem was a problem in common, when two or more video memory for a display was prepared in a graphic display device.

[0004] This invention aims at offering the image processor which can display two or more images on one screen in piles according to the image data memorized by each video memory, without being made in order to solve the above-mentioned technical problem in the conventional technique, and transmitting image data among two or more video memory.

[0005]

[Means for Solving the Problem and its Function] In order to solve an above-mentioned technical problem, the graphic display device of this invention Two or more image memory which memorizes two or more video signals, respectively, and an image control signal generating means to generate two or more read-out enabling signals which show the timing which reads two or more video signals from said two or more image memory, respectively, While giving two or more read-out control signals for reading said two or more video signals to said two or more image memory, respectively, corresponding respectively to said two or more read-out enabling signals The memory control means which generates two or more clock signals which synchronize with said two or more video signals read from said two or more image memory, respectively, A selection-signal generation means to generate the image selection signal for choosing switching one of said two or more of the video signals in two or more predetermined locations in the screen of said display, It has a display means to display an image according to a selection means to choose one of said two or more of the video signals, and one of said two or more of the clock signals according to the image selection signal given from said selection-signal generation section, and the video signal and clock signal which were chosen with said selection means.

[0006] According to the image data memorized, respectively, two or more images can be displayed on two or more image memory in piles on one screen, without transmitting image data among two or more image memory, since the clock signal corresponding to the selected video signal is chosen and a display means is supplied with a selection means, while choosing two or more video signals.

[0007] It has the memory area of the predetermined number of bits which two or more pixels contained in a field predetermined [on the screen of said display means] boil said selection-signal generation means, respectively, and corresponds. The memory which memorizes the image select data showing any of two or more of said video signals are chosen about each of two or more of said pixels, It is desirable to make it include a control signal supply means to supply the select data read-out control signal for reading said image select data from said memory as said image selection signal to said memory.

[0008] If it carries out like this, since the image select data memorized beforehand will be read to memory as an image selection signal, an image selection signal is easily generable.

[0009] Said control signal supply means may be a transfer way transmitted to said memory by making one of said two or more read-out control signals into said select data read-out control signal.

[0010] Since a select data read-out control signal is generated by the memory control means, the circuit of the dedication for generating a select data read-out control signal becomes unnecessary, and circuitry becomes easy.

[0011] You may make it said display means contain the D-A converter which changes into an analog video signal the digital video signal chosen with said selection means according to the clock signal chosen with said selection means.
[0012] If it carries out like this, since the clock signal which was suitable for each video signal, respectively will perform D-A conversion, an image can be expressed as good image quality.
[0013] You may make it said image control signal generating means include a means to generate the 1st signal which has the 1st period equivalent to the scan period of the one scanning line on the screen of said display means. Moreover, said memory control means is based on said 1st signal given from said image control signal generating means, and is N1 of said 1st period. The 1st PLL circuit which generates the 1st clock signal which has a twice (N1 is an integer) as many period as this, A level address-generation means to generate the level address of the 1st image memory which is one of said two or more of the image memory, By adding a perpendicular address-generation means to generate the perpendicular address of said 1st image memory, and said level address and said perpendicular address While the adder which generates the address given to said 1st image memory is included, you may make it said level address-generation means include the renewal means of the level address to which said level address is made to increase according to the pulse of said 1st clock signal.
[0014] Integer N1 set as the 1st PLL circuit If a value is changed, variable power of the image can be carried out horizontally.
[0015] While a graphic display device connects the processor in which arithmetic logical operation is still more possible, said processor, and said two or more image memory It has the bus which connects said processor and said memory control section. Said processor Said integer N1 in said 1st PLL circuit By changing a value, it is desirable that it is made to carry out variable power of the 1st image displayed on said display means by the 1st video signal read from said 1st image memory horizontally.
[0016] If it carries out like this, it will be an integer N1 by the processor. Variable power of the image can be horizontally carried out by changing a setup.
[0017] You may make it said image control signal generating means include a means to generate the 2nd signal which has the 2nd period equivalent to the scan period for one screen of said display means. Moreover, said 1st memory control means is further based on said 1st signal given from said image control signal generating means. A means to generate the 1st renewal signal of the scanning line which shows the timing equivalent to the termination of the scanning line about the 1st video signal read from said 1st image memory, It is based on either of said 1st and 2nd signals, and is N2 of said 2nd period. The 2nd PLL circuit which generates the 2nd renewal signal of the scanning line which has a twice (N2 is an integer) as many period as this is included. Said level address-generation means includes a means to reset said level address to predetermined initial value according to one pulse of said 1st renewal signal of the scanning line. Said perpendicular address-generation means Said pulse number of the 2nd renewal signal of the scanning line given according to one pulse of said 1st renewal signal of the scanning line between the two newest pulses of said 1st renewal signal of the scanning line, You may make it include a renewal means of the perpendicular address to update said perpendicular address, by adding the perpendicular address increment equivalent to the result of having carried out the multiplication of the difference of the address equivalent to a predetermined number in said display means of scanning lines to said perpendicular address.
[0018] Integer N2 set as the 2nd PLL circuit If a value is changed, variable power of the image can be carried out perpendicularly.
[0019] Said processor is said integer N2 in said 2nd PLL circuit. It may be made to carry out variable power of the 1st image displayed on said display means perpendicularly by changing a value with the 1st video signal read from said 1st image memory.
[0020] If it carries out like this, it will be an integer N2 by the processor. Variable power of the image can be perpendicularly carried out by changing a setup.
[0021]

[Example] Below, explanation is performed for the following sequence.
A. equipment whole configuration and actuation: — the configuration of B. image control signal generating section, and : of operation — the configuration of C. storage control section and the image storage section, and : of operation — various kinds of set point: at the time of enlarging or contracting of D. image — the configuration of E. animation write control section, and : of operation — the configuration of the F.3 port image storage section, and : of operation — G. modification: [0022] A. The whole equipment configuration and actuation : drawing 1 is the block diagram showing the configuration of a computer system equipped with the graphic display device as one example of this invention. The storage section 60, the image storage sections 61 and 62, and 3 port image storage section 63 are connected to the CPU bus 52 connected to CPU50. The control signal for reading a video signal serially is given to the three image storage sections 61, 62, and 63 from the storage control sections 71, 72, and 73, respectively. The 1st storage control section 71 supplies the still more nearly same control signal as the control signal given to the 1st image storage section 61 also to the storage section 60. This storage section 60 is the memory for memorizing the multiplexer signal MPX for choosing one of the video signals read from the three image storage sections 61–63. In addition, about the configuration and role of the four storage sections 60–63, it mentions later further.
[0023] The read–out port of 3 port image storage section 63 is connected to the 3rd storage control section 73, and the 1st write–in port is connected to the CPU bus 52, and the 2nd write–in port is connected to the animation write control section 74, respectively. As for the animation write control section 74, the image data of an animation are given, respectively from video–signal separation / digitization control section 76 and the animation data decompression section 78. video–signal separation / digitization control section 76 — a television tuner and a video play — since — while dividing the composite video signal given into a synchronizing signal and a component signal (an RGB code or YUV signal), a component signal is changed into a digital signal and the animation write control section 74 is supplied. On the other hand, the animation data decompression section 78 elongates the compression image data contained by CD–ROM, a hard disk, a magneto–optic disk, etc., and supplies it to the animation write control section 74. The animation write control section 74 writes the image data of the supplied animation in 3 port image storage section 63. In addition, about the internal configuration of the animation write control section 74, and actuation, it mentions later further.
[0024] This computer system is further equipped with the image control signal generating section 80, the video–signal change–over section 82, the clock signal change–over section 84, the D–A conversion section 86, the amplifier 88, and the color monitor 90. The image control signal generating section 80 generates the image control signals [1–HPIE / VPIE and / 3] 1–3 for directing the timing of read–out of a video signal, and supplies them to the three storage control sections 71–73. one of the video signals 01–RGB 03 with which the video–signal change–over section 82 was read from the three image storage sections 61–63 — it chooses and the D–A conversion section 86 is supplied. Moreover, the clock signal change–over section 84 chooses one of the clock signals 1–CLK 3 outputted from the three storage control sections 71–73, and supplies it to the D–A conversion section 86 as a synchronizing signal of D–A conversion. The multiplexer signal MPX given to the video–signal change–over section 82 and the clock signal change–over section 84 is given from the storage section 60.
[0025] The D–A conversion section 86 changes into analog signals AR, AG, and AB digital signal RGB0 which is 24 bits to which 8 bits was assigned for every color of RGB. These analog signals AR, AG, and AB are amplified in an amplifier 88, respectively, and are given to a color monitor 90. In addition, Vertical Synchronizing signal VSYNC and Horizontal Synchronizing signal HSYNC of a color monitor 90 are given from the image control signal generating section 80.
[0026] Drawing 2 is the explanatory view showing the relation between the room of the four storage sections 60–63, and a screen display. The size of each storage section is the vertical number Wv of Rhine. Several Whs horizontal pixel The number of bits Nb assigned to each pixel A definition can be given. The storage section 60 supports the screen of 1600 pixel x1200 line, and has a depth of 2 bits.

The multiplexer data memorized by the storage section 60 are given to the video-signal change-over section 82 and the clock signal change-over section 84 as a multiplexer signal MPX. Therefore, the depth of the storage section 60 is set as the number of bits which can identify mutually the maximum number of the image storage section which can be carried in this computer system. Since the three image storage sections are prepared in the example of drawing 1 , the storage section 60 is good in a depth of 2 bits.

[0027] As shown in drawing 2 (B), the 1st image storage section 61 supports the screen of 1600 pixel x1200 line, and has a depth of 24 bits. The image data memorized by the image storage section 61 are full color natural image data. In addition, three memory with a depth of 8 bits may be used as the image storage section 61.

[0028] It carries out [each other / corresponding to the screen of the magnitude with same storage section 60 and 1st image storage section 61], is, and has room. The storage control section 71 (drawing 1) supplies the same read-out signal as the storage section 60 and the image storage section 61, and the multiplexer signal MPX and video signal RGB 01 equivalent to the same display position are read from the storage section 60 and the image storage section 61, respectively.

[0029] The 2nd image storage section 62 supports the screen of 640 pixel x400 line, and has a depth of 24 bits. Moreover, 3 port image storage section 63 supports the screen of 800 pixel x600 line, and has a depth of 24 bits. In addition, the three image storage sections 61-63 may support the screen of the same magnitude. Each of the storage control sections 71-73 reads video signals 01-RGB 3 from the image storage sections 61-63 according to the read-out enabling signals [1-HPIE / VPIE and / 3] 1-3 given from the image control signal generating section 80, respectively.

[0030] Drawing 3 (A) is the explanatory view showing the address map about three OS's using the three image storage sections. The three image storage sections are managed by three different OS's (multi-OS, OS1, OS2), respectively. Multi-OS has the function which switches management of a system to other OS's temporarily. Moreover, each OS has the memory area of the image storage sections 61-63, respectively. ** of drawing 3 (A) - ** show the procedure of a change of OS. First, if the directions which require the change to OS1 from multi-OS are inputted from a keyboard 40 or a mouse 42, the directions will be given to multi-OS from BIOS (procedure **), and multi-OS will switch management of a system to OS1 (procedure **). OS1 switches management of a system to multi-OS again, after performing directed processing and completing processing (procedure **). And the image memorized by each image storage sections 61-63 is displayed on a color monitor 90 through BIOS (procedure **).

[0031] Drawing 3 (B) is the top view showing the condition that the image of each image storage sections 61-63 was displayed on the color monitor 90. In addition, it is also possible to manage the two image storage sections by one OS, without using two or more OS's. For example, the same OS is able to manage the three image storage sections 61-63.

[0032] Drawing 4 is the explanatory view showing relation with a screen display in the read-out enabling signals [1-HPIE / VPIE and / 3] 1-3 and color monitor 90 which are outputted from the image control signal generating section 80. The viewing areas W01, W02, and W03 of three images displayed on the color monitor 90 according to three video signals RGB01-RGB03 read from the three image storage sections 61-61, respectively are shown in the upper left of drawing 4 .

[0033] The signal wave form on X1-X2 line is shown in the lower part of drawing 4 , and the wave of the horizontal component HMPX of Horizontal Synchronizing signal HSYNC, the horizontal read-out enabling signals 1-HPIE 3 given to the three storage control sections 71-73 from the image control signal generating section 80, respectively, and the multiplexer signal read from the storage section 60 is shown in it. On the other hand, the signal wave form on Y1-Y2 line is shown in the right-hand side of drawing 4 , and the wave of the vertical component VMPX of Vertical Synchronizing signal VSYNC, the perpendicular read-out enabling signals 1-VPIE 3 given to the three storage control sections 71-73 from the image control signal generating section 80, respectively, and the multiplexer signal read from the storage section 60 is shown in it.

[0034] The horizontal read-out enabling signal HPIE1 given to the 1st image storage section 61 is maintained at H level in the viewing area to the left end location A of a color monitor 90 - the right end location F. Moreover, the perpendicular read-out enabling signal VPIE1 is also maintained at H level in all the fields of the perpendicular direction of a screen. Consequently, the 1st video signal RGB 01 is read from the 1st image storage section 61 in the period these read-out enabling signals HPIE1 and VPIE1 of whose are all H level. Similarly, the 2nd video signal RGB 02 is read from the 2nd image storage section 62 in the period whose read-out enabling signals HPIE2 and VPIE2 are all H level, and the 3rd video signal RGB 03 is read from the 3rd image storage section 63 in the period whose read-out enabling signals HPIE3 and VPIE3 are all H level.
[0035] The video-signal change-over section 82 chooses and outputs one of the three video signals 01-RGB 3 according to the multiplexer signal MPX outputted from the storage section 60. Like the 1st video signal RGB 01, although the multiplexer signal MPX is a signal which shows the value of the multiplexer data in each pixel according to the scan of a color monitor 90, by drawing 4 , it separates into change of the horizontal component HMPX after [expedient] illustrating, and change of a vertical component VMPX, and it is drawn. In other words, the actual multiplexer signal MPX is a signal with which the same signal as a horizontal component HMPX is continuing in order of the scanning line.
[0036] On the X1-X2 line of drawing 4 , the value of the horizontal component HMPX of the multiplexer signal MPX is changing in order of 1, 2, 3, and 1, and video signals RGB01, RGB02, RGB03, and RGB01 are chosen according to this, respectively.
[0037] In addition, according to size, a location, etc. of each image field which were specified on the screen of a color monitor 90, CPU50 determines the multiplexer data memorized by the storage section 60. That is, if an operator specifies the 2nd, the size of the 3rd viewing area W02 and W03, a location, and vertical relation using a keyboard or a mouse, according to this assignment, CPU50 will generate multiplexer data and will write in the storage section 60. In addition, the image displayed on the 1st viewing area W01 is a fundamental image, and this viewing area W01 is being fixed to predetermined magnitude.
[0038] in case the image of different size as shown in drawing 2 (B), (C), and (D) is displayed, it usually comes out that a mutually different synchronizing signal (a Horizontal Synchronizing signal and Vertical Synchronizing signal) for which was resembled, respectively and it was suitable is used. Therefore, it is usually impossible to display in piles the video signal read from each image storage sections 61-63 on the same screen. So, in this computer system, as shown in drawing 1 , the clock signals CLK1, CLK2, and CLK3 which synchronize with the video signal read from each image storage sections 61-63, respectively are given to the clock signal change-over section 84 from the storage control sections 71, 72, and 73, and the clock signal change-over section 84 chooses one of the clock signals of these according to the multiplexer signal MPX read from the storage section 60, and supplies it to the D-A conversion section 86. Therefore, the D-A conversion section 86 can perform D-A conversion according to the clock signal which synchronized with the video signal outputted from the video-signal change-over section 82. Thus, since D-A conversion of the video signal read from each image storage sections 61-63 is carried out by the clock signals CLK1, CLK2, and CLK3 which synchronized with each, the analog video signals AR, AG, and AB outputted from the D-A conversion section 86 turn into a signal which reproduces an image faithfully.
[0039] As mentioned above, according to this computer system, since an image is displayed for one of the video signals 01-RGB 3 read from the three image storage sections 61-63 with a change in the video-signal change-over section 82, CPU50 does not need to perform processing which transmits image data among the image storage sections 61-63, and where two or more images are piled up, it can display on a high speed. Under the present circumstances, since D-A conversion is performed according to the clock signal corresponding to each video signal, two or more images corresponding to a different screen size are faithfully reproducible.
[0040] moreover, since the room of the storage section 60 and the image storage section 61 supports

the same screen size, it can set on the screen of a color monitor 90 — each — there is an advantage that the multiplexer data memorized in the storage section 60 can be easily set up according to assignment of the size of image field W01–3, a location, and vertical–related.

[0041] In addition, when OS which manages the three image storage sections 61–63 is a multi–window system, each OS is able to display two or more windows in piles in each image fields W01 and W02 and W03.

[0042] B. The configuration and actuation of the image control signal generating section : drawing 5 is the block diagram showing the internal configuration of the image control signal generating section 80. Moreover, the timing chart drawing 6 indicates horizontal actuation of the image control signal generating section 80 to be, and drawing 7 are timing charts which show vertical actuation. As shown in drawing 5 , the image control signal generating section 80 generates Horizontal Synchronizing signal HSYNC supplied to a color monitor 90 and Vertical Synchronizing signal VSYNC, and the level read–out enabling signal HPIE supplied to the three storage control sections 71–73, respectively and the perpendicular read–out enabling signal VPIE. The image control signal generating section 80 is equipped with the following component.

[0043] DPLL section 100: Generate the dot clock signal DTCLK for synchronizing each part in the image control signal generating section 80.

[0044] Horizontal–synchronization period counter 111: Based on the dot clock signal DTCLK, as shown in drawing 6 (a), generate the signal H1 which serves as L level in the horizontal synchronization period HS. Here, Horizontal Synchronizing signal HSYNC is the period maintained at L level in the horizontal synchronization period HS. In addition, the output signal H1 of a counter 111 is outputted to the exterior of the image control signal generating section 80 as Horizontal Synchronizing signal HSYNC as it is so that drawing 5 may show. In other words, a counter 111 is a circuit which creates Horizontal Synchronizing signal HSYNC. The data in which the die length of the period when a signal H1 serves as L level is shown are written in the register which is not illustrated in the horizontal synchronization period counter 111 from CPU50 through the CPU bus 52. In addition, the die length of a period is expressed with the pulse number of the dot clock signal DTCLK. It is common to each counter explained below that the die length of a period is set up by CPU50. Once a signal H1 starts on H level, it will be maintained at H level until the horizontal synchronization period counter 111 is reset by the reset signal H5 given from the level reset counter 115 mentioned later.

[0045] Level back–porch period counter 112: It is reset by the reset signal H5, fall to L level, and generate the signal H2 (drawing 6 (b)) which starts on H level at the telophase of the level back porch period HB. Here, the level back porch period HB is a period of the ** term of the standup of Horizontal Synchronizing signal HSYNC to the image shelf–life HE.

[0046] Level image shelf–life counter 113: It is reset by the reset signal H5, fall to L level, and generate the signal H3 (drawing 6 (c)) which starts on H level at the telophase of the level image shelf–life HE.

[0047] By the way, as shown in drawing 5 , the signal H2 and the reversal signal of a signal H3 are inputted into the AND gate 116. The output signal HYENB of the AND gate 116 is a signal which serves as H level in the level image shelf–life HE, as shown in drawing 6 (h). Below, Signal HYENB is called a "horizontal effective enable signal." Horizontal effective enable signal HYENB is able to display an effective image on a color monitor 90 only in the period of H level. In addition, the level image shelf–life HE is a period equivalent to the 1st image field W01 which is to a base, and is a period equivalent to all the range of the image field W01 shown in drawing 4 (the range of a location A – a location F).

[0048] Level front–porch period counter 114: Fall to L level according to a reset signal H5, and generate the signal H4 (drawing 6 (d)) which starts on H level at the telophase of the level front porch period HF. Here, the level front porch period HF is a period of the ** term of the telophase of the level image shelf–life HE to the level reset period HR (period for one clock of the dot clock signal DTCLK).

[0049] Level reset period counter 115: Generate the reset signal H5 (drawing 6 (e)) which resets the above–mentioned counters 111–114. A signal H5 is a signal which falls to L level in the standup of the

next dot clock signal DTCLK of Ushiro to whom the output signal H4 of the level front porch period counter 114 started, and starts again after 1 clock. As mentioned above, counters 111–114 are reset by falling of a signal H5, and signals H1–H4 fall to L level.

[0050] As mentioned above, while Horizontal Synchronizing signal HSYNC is generated by work of counters 111–115, each horizontal period is specified.

[0051] The image control signal generating section 80 has the counters 121–125 corresponding to each counters 111–115 mentioned above as a counter which specifies a vertical period, respectively. Everything but making Horizontal Synchronizing signal HSYNC (= H1) into clocked into instead of the dot clock signal DTCLK of the counters 121–125 which specify a vertical period is the same as that of the counters 111–115 which specify a horizontal period. You can understand this, if the wave of the signals H1–H5 which show the wave of the output signals V1–V5 of the counters 121–125 shown in drawing 7 (a) – (e) to drawing 6 (a) – (e) is compared. However, CPU50 differs from the die length of the period set as each of the horizontal counters 111–114, and the die length of the period set as each of the vertical counters 121–124.

[0052] Moreover, corresponding to the AND gate 116 which creates level effective enable signal HYENB, the AND gate 126 which creates perpendicular effective enable signal VYENB (drawing 7 (h)) is also formed.

[0053] The image control signal generating section 80 is equipped with three enabling–signal generation circuits 131–133 for creating further the read–out enabling signals HPIE and VPIE given to the three storage control sections 71–73, respectively. Each of the enabling–signal generation circuits 131–133 is equipped with the following component.

[0054] Level display initiation period counter 134: Reset is canceled in the standup of level effective enable signal HYENB (drawing 6 (h)), the signal H6 (drawing 6 (i)) which starts on H level at the ** term of a level viewing–area period is generated, and it is again reset in falling of level effective enable signal HYENB. Here, a level viewing–area period means the period when an image is displayed on a color monitor 90 according to the image data memorized by the image storage section. In drawing 4 , the level viewing–area period of the image field W01 is a period of a location A – a location F, and the period of a location B – a location D and the level viewing–area period of the image field W03 of the level viewing–area period of the image field W02 are periods of a location C – a location E.

[0055] Level viewing–area period counter 135: Reset is canceled in the standup of level effective enable signal HYENB, the signal H7 (drawing 6 (j)) which starts on H level at the telophase of a level viewing–area period is generated, and it is again reset in falling of level effective enable signal HYENB.

[0056] AND gate 136: Generate the horizontal read–out enabling signal HPIE (drawing 6 (k)) by taking the AND of a signal H6 and the reversal signal of a signal H7.

[0057] The enabling–signal generation circuits 131–133 are further equipped with the two above–mentioned counters 134,135 related horizontally, two counters 137,138 respectively corresponding to the AND gate 136, and AND gates 139 about the perpendicular direction. From the AND gate 139, the perpendicular read–out enabling signal VPIE (drawing 7 (k)) is outputted. In addition, to the counter 134,135 related horizontally making the dot clock signal DTCLK clocked into, and making horizontal effective enable signal HYENB into reset input, the counter 137,138 about a perpendicular direction makes clocked into Horizontal Synchronizing signal HSYNC (= H1), and makes perpendicular effective enable signal VYENB reset input.

[0058] The image control signal generating section 80 is equipped with a number equal to the number of the image storage sections 61–63 of enabling–signal generation circuits 131–133. Namely, the group (HPIE1, VPIE1) of each read–out enabling signal shown in drawing 4 , (HPIE2, VPIE2), and (HPIE3, VPIE3) are generated by the enabling–signal generation circuits 131–133 corresponding to each image storage sections 61–63, respectively.

[0059] In addition, the pulse number specified to each period by CPU50 is set to the counter 134,135,137,138 in the enabling–signal generation circuit 131–133. According to the size, the location,

and vertical relation of each image fields W01–W03 (drawing 4) which the operator specified on the screen of a color monitor 90, CPU50 determines these pulse numbers.

[0060] As explained above, the image control signal generating section 80 generates Horizontal Synchronizing signal HSYNC, Vertical Synchronizing signal VSYNC, and the read–out enabling signals HPIE and VPIE 1–3 [1–] 3 which are shown in drawing 4 . As shown in drawing 1 , Horizontal Synchronizing signal HSYNC and Vertical Synchronizing signal VSYNC are supplied to a color monitor 90, and the enabling signals [1–VPIE / HPIE and / 3] 1–3 are supplied to the storage control sections 71–73.

[0061] C. The configuration and actuation of the storage control section and the image storage section : here, explain the configuration and actuation of the storage control sections 71 and 72 and the image storage sections 61 and 62. About the configuration and actuation of 3 port storage control section 73 and 3 port image storage section 63, it mentions later.

[0062] Drawing 8 is the block diagram showing the internal configuration of the storage control section 71. Moreover, drawing 9 is a timing chart which shows actuation of the storage control section 71. The storage control section 71 is equipped with the H–PLL section 141, the V–PLL section 142, the three waveform–shaping sections 143–145, NAND gates 146, inverters 147, and address–generation circuits 148.

[0063] The H–PLL section 141 is Nh of the frequency of the horizontal read–out enabling signal HPIE. It is the PLL circuit which generates the clock signal CLK (drawing 9 (h)) which has a twice as many frequency as this. Here, it is Nh. It is the number of pixels equivalent to one period of the horizontal read–out enabling signal HPIE. This number Nh of pixels Several Whs horizontal pixel of the image storage sections 61–63 shown in drawing 2 (B), (C), and (D) It can be set as a different value. CPU50 is Nh of the H–PLL section 141. By changing a value, it is Nh. Wh According to relation, an image can be expanded horizontally or it can reduce. About the zooming function of such an image, it mentions later further. In addition, in the H–PLL section 141, the phase of a clock signal CLK is locked synchronizing with the leading edge of the horizontal read–out enabling signal HPIE.

[0064] The V–PLL section 142 is Nv of the frequency of the perpendicular read–out enabling signal VPIE. It is the PLL circuit which generates the signal VCLK (drawing 9 (b)) which has a twice as many frequency as this. Here, it is Nv. It is the number of Rhine equivalent to one period of the perpendicular read–out enabling signal VPIE. This number Nv of Rhine The number Wv of Rhine of the image storage sections 61–63 shown in drawing 2 (B), (C), and (D) It can be set as a different value and is Nv. Wv According to relation, zooming of the image can be carried out perpendicularly.

[0065] Drawing 10 is the block diagram showing the internal configuration of the waveform–shaping section 143,144,145. Each waveform–shaping section consists of two D flip–flops 151,152 and the AND gates 153. The clock signal CLK generated in the H–PLL section 141 is inputted into the clock input terminal of two D flip–flops 151,152. The input signal to the waveform–shaping section is given to D input terminal of 1st D flip–flop 151. The output of 1st D flip–flop 151 is given to the 2nd D input terminal and AND gate 153 of D flip–flop 152. The reversal output of the 2nd flip–flop 152 is further given to the AND gate 153.

[0066] Drawing 11 is a timing chart which shows actuation of the waveform–shaping section. The input signals of the three waveform–shaping sections 143–145 shown in drawing 8 are VPIE, HPIE, and /VCLK, respectively. Here, the notation "/" attached before VCLK shows that Signal VCLK is a signal reversed with the inverter 147. After the input signal VPIE to the waveform–shaping section 143,144,145, /VCLK, and HPIE start so that drawing 11 may show, each output signal VCLR, INC, and HCLR starts on H level in falling of the 1st clock signal CLK, and an output signal falls to L level by the 2nd negative going edge.

[0067] As shown in drawing 8 , the clock signal CLK generated in the H–PLL section 141 is given in common to the clock input terminal of the three waveform–shaping sections 143–145. Perpendicular reset–signal VCLR generated in the 1st waveform–shaping section 143 is a signal which change of one pulse generates whenever the display for one screen of an image field is completed.

[0068] Level reset-signal HCLR generated in the 2nd waveform-shaping section 144 is a signal which change of one pulse generates whenever the display of scanning-line 1 duty is completed.
[0069] The perpendicular increment signal INC generated in the 3rd waveform-shaping section 145 is a signal which change of one pulse generates whenever read-out of the image data of scanning-line 1 duty is completed. In addition, level reset-signal HCLR and the perpendicular increment signal INC are later mentioned about this, although it has an important role in case zooming of the perpendicular direction of an image is performed.
[0070] NAND gate 146 (drawing 8) takes the output Q151 (drawing 10) of 1st D flip-flop 151 of the 2nd waveform-shaping section 144, and an AND with the perpendicular enabling signal VPIE, and generates the lead enable signal RE.
[0071] In addition, the output signals VCLR and HCLR of the 1st storage control section 61, and INC, RE and CLK are given common to the image storage section 61 and the storage section 60.
[0072] The three storage control sections 71-73 shown in drawing 1 have the same configuration shown in drawing 8 , respectively. However, the number Nh of pixels set as the H-PLL section 141 A value and the number Nv of Rhine set as the V-PLL section 142 A value changes mutually with each storage control sections. This is explained in full detail in explanation of enlarging-or-contracting processing of an image.
[0073] Drawing 12 is the block diagram showing the internal configuration of the two image storage sections 61. The image storage section 61 has random read-out / write control section 160, the serial read-out control section 161, and memory 162. The same of this configuration is said of the storage sections 60 and 62.
[0074] The input of random read-out / write control section 160 is as follows.
The address / data shared bus of the ADBUS:CPU bus 52.
AHLRW: The signal which shows selection of the high order/low order of the address, and selection of data read-out / data store.
AEN: A thing **** signal with an effective address bus.
DEN: The signal which shows that a data bus is effective.
[0075] The output of random read-out / write control section 160 is as follows.
RADDRS: Random address.
RDATA: Random data.
RWR: A random write-in signal.
RRD: Random read-out signal.
[0076] The I/O of the serial read-out control section 161 is as follows.
ADBUS: Address bus.
ADSEL: The address selection signal which chooses one of the 4 ** addresses.
AEN: The address valid signal which shows that an address bus ADBUS is effective.
VCLR: The perpendicular reset signal which change of one pulse generates whenever the display of one batch of an image field is completed.
INC: The perpendicular increment signal which change of one pulse generates whenever read-out of the image data of scanning-line 1 duty is completed.
HCLR: The level reset signal which change of one pulse generates whenever the display of scanning-line 1 duty is completed.
CLK: Clock signal.
RE: Lead enable signal.
SADDRS: Serial address.
SRD: Serial read-out enabling signal
[0077] Drawing 13 is the block diagram showing the internal configuration of the memory 162 shown in drawing 12 . Memory 162 is equipped with the memory cell array 165, a selector 166, and two 3 State buffer sections 167,168. A selector 166 connects one side of the random address RADDRS and the

serial address SADDRS to the address input terminal of the memory cell array 165 according to the random write-in signal RWR. From the output terminal of the memory cell array 165, the random data RDATA are outputted through 1st 3 State buffer section 167. The random read-out signal RRD is given to the control terminal of 1st 3 State buffer section 167. Further, the output of the memory cell array 165 is outputted as a video signal RGB 01 from 2nd 3 State buffer section 168, and is given to the video-signal change-over section 82 (drawing 1). The serial data read-out enabling signal SRD given from the serial read-out control section 161 is given to the control input terminal of 2nd 3 State buffer section 168. In addition, in order to display an animation on a high speed, it is desirable to use the memory cell array 165 which consisted of static RAMs.

[0078] Drawing 14 is the block diagram showing the internal configuration of the serial read-out control section 161 shown in drawing 12 . Moreover, drawing 15 is a timing chart which shows actuation of the serial read-out control section 161. The serial read-out control section 161 is equipped with four 8-bit address registers 171-174 and decoders 176, respectively. A decoder 176 decodes the 2-bit address selection signal ADSEL, and makes enabling state every four address registers [one] 171-174 one by one (drawing 15 (b)). Sequential maintenance of the address AH given from the address bus ADBUS, AL, BH, and the BL (drawing 15 (a)) is carried out at each register by the leading edge of the address valid signal AEN given to address registers 171-174.

[0079] Drawing 16 is the conceptual diagram showing the relation of the screen and the address corresponding to memory. Address AHAL is the address (it is hereafter called the "starting point address") which shows the reference point Pi at the upper left of the field displayed with image data. Moreover, Address BHBL is the increment (it is hereafter called the "addition address") of the address equivalent to the die length of the scanning line of a screen. In addition, in interlacing, the addition address BHBL serves as a value according to the rate of an interlace. For example, in interlacing 2:1, the addition address BHBL serves as address increment equivalent to one twice the die length of the scanning line.

[0080] Further, as a circuit which calculates the address according to a scan, the serial read-out control section 161 (drawing 14) is equipped with three adders 180,182,184, two latches 186,188, and level counters 190, and is equipped with the four AND gates 192,194,196,198. The adder 180,184 and the latch 186,188 constitute the circuit which computes the vertical address among these. Moreover, the level counter 190 constitutes the circuit which computes the horizontal address.

[0081] An adder 184 adds the 16-bit addition address BHBL held at two address registers 173,174, and the 1st latch's 186 output D186. The 1st latch 186 is reset by the leading edge of the output signal of the 1st AND gate 192, and holds the output Q184 of an adder 184 by the leading edge of the output signal of the 2nd AND gate 194. Since the 1st AND gate 192 has taken the AND of perpendicular reset-signal VCLR and a clock signal CLK, as it is shown in drawing 15 (j), the 1st latch 186 is reset by the leading edge of the clock signal CLK generated at the period when perpendicular reset-signal VCLR is maintained at H level. Moreover, since the 2nd AND gate 194 has taken the AND of the perpendicular increment signal INC and a clock signal CLK, the 1st latch 186 holds the output Q184 of an adder 184 by the leading edge of the clock signal CLK generated at the period when the perpendicular increment signal INC is maintained at H level.

[0082] Since the 1st latch's 186 output Q186 is fed back to the adder 184, whenever the 1st latch 186 holds new data (i.e., whenever the pulse of the perpendicular increment signal INC occurs), the output Q184 of an adder 184 increases only the addition address BHBL (drawing 15 (i)).

[0083] The 2nd latch 188 is reset by the leading edge of the output signal of the 1st AND gate 192, and holds the 1st latch's 186 output Q186 by the leading edge of the output signal of the 3rd AND gate 196. Since the 3rd AND gate 196 has taken the AND of level reset-signal HCLR and a clock signal CLK, as it is shown in drawing 15 (k), the 2nd latch 188 holds the 1st latch's 186 output Q186 by the leading edge of the clock signal CLK generated at the period when level reset-signal HCLR is maintained at H level.

[0084] The 1st adder 180 adds the starting point address AHAL held at the 2nd latch's 188 output Q188,

and two address registers 171,172. The output Q180 of the 1st adder 180 is equivalent to the vertical address.

[0085] The level counter 190 is reset by the leading edge of the output signal of the 3rd AND gate 196, and performs count-up by the leading edge of the output signal of the 4th AND gate 198. Since the 4th AND gate 198 has taken the AND of the reversal signal and clock signal CLK of the lead enable signal RE, as it is shown in drawing 15 (l), according to the leading edge of the clock signal CLK generated at the period when the lead enable signal RE is maintained at H level, the level counter 190 performs count-up. In addition, the counted value Q190 of the level counter 190 is equivalent to the horizontal address.

[0086] The 2nd adder 182 adds the output Q180 of the 1st adder 180, and the counted value of the level counter 190. The output Q182 of an adder 182 is equal to the result of having added the starting point address AHAL, latch's 188 output Q188 (drawing 15 (k)), and the counted value Q190 (drawing 15 (l)) of the level counter 190. The output 182 of this adder 182 is given to memory 162 as the serial address SADDRS. As shown in drawing 15 (m), after the serial address SADDRS becomes the value of the sum of the starting point address AHAL and the addition address BHBL, the increment of it is carried out one [at a time] synchronizing with the leading edge of a clock signal CLK. Therefore, the image data RGB 01 which contain a RGB component from memory 162 according to this serial address SADDRS are read serially.

[0087] The serial read-out control section 161 (drawing 14) is further equipped with D flip-flop 199. The lead enable signal RE is given to D input terminal of D flip-flop 199, and the clock signal CLK is given to the clock input terminal. The output of D flip-flop 199 is the serial data read-out enabling signal SRD (drawing 15 (o)). The serial data read-out enabling signal SRD falls to L level in falling of the next clock signal CLK of Ushiro from whom the lead enable signal RE fell to L level. As shown in drawing 13 , since the serial data read-out enabling signal SRD is given to the control terminal of 3 State buffer 168, only in the condition that Signal SRD fell to L level, the image data RGB 01 are read from memory 162. That is, as shown in drawing 15 (m) and (n), the value of Address SADDRS shows the location (pixel location [directly under] of the address origin/datum Pi shown in drawing 16 (A)) shown by (AHAL+BHBL), and read-out of image data is started from this location. Therefore, the image of the address reference point Pi is not displayed.

[0088] In addition, the clock signal CLK is created by the H-PLL section 141 (drawing 8), and the phase of the negative going edge of a clock signal CLK is locked by the leading edge of the horizontal read-out enabling signal HPIE (drawing 9). Generally, since the lock of the phase by the PLL circuit is not perfect, gap (jitter) of some may arise in the phase of a clock signal CLK. However, since serial read-out of image data is controlled by the leading edge of a clock signal CLK to be shown in drawing 15 , even if a jitter arises in a clock signal CLK, a problem does not arise in read-out of data.

[0089] Drawing 17 is a timing chart which shows actuation of the serial read-out control section 161 at the time of perpendicular direction expansion of an image. However, drawing 17 shows only change of the main signals related to renewal of the vertical address among the signals shown in drawing 15 . Whenever one pulse of perpendicular increment signals INC occurs, only BHBL increases the output Q184 of an adder 184. On the other hand, whenever one pulse of level reset-signal HCLR(s) occurs, only BHBL increases latch's 186 output Q186. At time of day t1, since the pulse of the perpendicular increment signal INC has not occurred among the two newest pulses of level reset-signal HCLR, the value of of latch 188 output Q188 is maintained as it is. Thus, period Tv of the perpendicular increment signal INC In being bigger than the period Tv0 of level reset-signal HCLR, latch's 188 output Q188 (namely, value of the perpendicular address) changes so that the case where the same value is repeated may be included, as shown in drawing 17 (f). Level reset-signal HCLR(s) are Horizontal Synchronizing signal HSYNC given to a color monitor 90 and a signal which has the same frequency, and are signals generated one pulse whenever the scanning line on a screen is updated. If latch's 188 output Q188 changes as shown in drawing 17 (f), as shown in drawing 16 (B), the image on the same scanning line

memorized by memory will be repeatedly displayed in the screen of a color monitor 90, consequently an image will be expanded perpendicularly.
[0090] In addition, the scale factor of the perpendicular direction at the time of an image being displayed on a color monitor 90 is the period Tv0 of level reset-signal HCLR, and the period Tv of the perpendicular increment signal INC. It is given by the ratio (Tv / Tv0). Period Tv of the perpendicular increment signal INC The set point Nv of the V-PLL section 142 (drawing 8) It is adjusted by changing.
[0091] Drawing 18 is a timing chart which shows actuation of the serial read-out control section 161 at the time of perpendicular direction contraction of an image. At time of day t2, since two pulses of the perpendicular increment signal INC have occurred among the two newest pulses of level reset-signal HCLR, the address BHBL twice the value of addition is added to latch's 188 output Q188. Thus, period Tv of the perpendicular increment signal INC In being smaller than the period Tv0 of level reset-signal HCLR, latch's 188 output Q188 changes like drawing 18 (f) so that some of values (the example of drawing 18 BHBLx 4) of an integral multiple may be skipped to the addition address BHBL. Consequently, as shown in drawing 16 (C), the image on the scanning line of what book memorized by memory is not displayed in the screen of a color monitor 90, but an image is reduced perpendicularly.
[0092] As shown in drawing 17 and drawing 18 , the value with which the serial read-out control section 161 is equivalent to the result to which level reset-signal HCLR carried out the multiplication of the addition address BHBL to 1 pulse ********** and the pulse number of the perpendicular increment signal INC given between the two newest pulses of level reset-signal HCLR is added to latch's 188 output Q188 (namely, perpendicular address). Therefore, like [in the case of the time of day t1 of drawing 17], when the pulse of the perpendicular increment signal INC has not generated one among the two newest pulses of level reset-signal HCLR, the perpendicular address Q188 is maintained at a value as it is. On the other hand, like the time of day t2 of drawing 18 , when two pulses of the perpendicular increment signal INC have occurred among the two newest pulses of level reset-signal HCLR, the address BHBL twice the value of addition is added to the perpendicular address Q188.
[0093] in addition, the scale factor in the case of also expanding the scale factor in the case of reducing an image perpendicularly — the same — the period Tv0 of level reset-signal HCLR, and period Tv of the perpendicular increment signal INC It is given by the ratio (Tv / Tv0).
[0094] D. Various kinds of set points at the time of enlarging or contracting of an image : it is possible to be able to carry out zooming of the image, and also to change the location and size of each image fields W01-W03 (drawing 4) in this computer system. In addition, zooming of an image is realized by work of the H-PLL section 141 of the storage control sections 71-73 (drawing 1 , drawing 8), the V-PLL section 142, and the serial read-out control section 161 (drawing 14), and modification of the location of an image field or size is realized by work of the enabling-signal generation circuits 131-133 (drawing 5) corresponding to each image field.
[0095] Drawing 19 is the explanatory view showing the storage control section 71 (drawing 8) at the time of displaying only the image memorized by the 1st image storage section 61, and various kinds of set points of an enabling-signal generation circuit (drawing 5).
[0096] In drawing 19 (A), the horizontal period of the signal about the image field W01 is classified into the horizontal synchronization period HS, the level back porch period HB and the level image shelf-life HE, and the level front porch period HF and the level reset period HR, as explained also in drawing 6 . The set point Nh0 of the H-PLL section 141 (drawing 8) of the 1st storage control section 71 is equal to the total value (HS+HB+HE+HF+HR) of the value which expressed these periods with the number of pixels. In addition, the level image shelf-life HE of the 1st image field W01 is 1600 pixels. One pulse of the clock signal CLK created in the H-PLL section 141 is equivalent to 1 pixel at the time of reading a video signal serially so that the timing chart of drawing 15 may also show. The frequency fh0 of this clock signal CLK is equal to the value which multiplied the frequency of the horizontal read-out enabling signal HPIE1 over the basic image field W01, i.e., the frequency of Horizontal Synchronizing signal HSYNC given to a color monitor 90 from the image control signal generating section 80, by the set point

Nh0 of the H-PLL section 141. In this example, it is 0= 100MHz of fh(s).

[0097] The set point Nv0 of the V-PLL section 142 of the 1st storage control section 71 is equal to the total value (VS+VB+VE+VF+VR) of the value which expressed the perpendicular back porch period VB, the perpendicular image shelf-life VE and the perpendicular front porch period VF, and the perpendicular reset period VR with the number of Rhine, respectively. [the vertical-synchronization period VS,] In addition, the perpendicular image shelf-life VE of the 1st image field W01 is 1200 lines. The frequency fv0 of the perpendicular increment signal INC generated in the V-PLL section 142 is equal to the value which multiplied the frequency of the perpendicular read-out enabling signal VPIE1 of the basic image field W01, i.e., the frequency of Vertical Synchronizing signal VSYNC given to a color monitor 90 from the image control signal generating section 80, by the set point Nv0 of the V-PLL section 142. In this example, it is 0= 80kHz of fv(s).

[0098] The set point of four counters 134,135,137,138 contained in the 1st enabling-signal generation circuit 131 (drawing 5) is used in order to specify the 1st location and size of the image field W01. The value of the set point Kh1 of the level display initiation period counter 134 and the set point Kv1 of the perpendicular display initiation period counter 137 is zero about the 1st image field W01 used as a base.

[0099] The set point Kh2 of the level viewing-area period counter 135 is a value which expressed the level image shelf-life HE with the pulse number of the dot clock signal DTCLK (drawing 5). As for the frequency of the dot clock signal DTCLK, it is desirable to be set as the same frequency (= 100MHz) as the horizontal clock signal CLK1 (drawing 8 , drawing 15) over the 1st image field W01 used as a base. When the frequency of the dot clock signal DTCLK and the frequency of a clock signal CLK1 are equal, the set point Kh2 of a counter 135 is equal to the number of pixels of the level image shelf-life HE (= 1600).

[0100] The set point Kv2 of the perpendicular viewing-area period counter 138 is a value which expressed the perpendicular image shelf-life VE with the pulse number of Horizontal Synchronizing signal HSYNC. Since the frequency of Horizontal Synchronizing signal HSYNC has the same frequency (= 80kHz) as the perpendicular increment signal INC1 (drawing 8 , drawing 15) over the basic image field W01 as mentioned above, the set point Kv2 of a counter 138 is equal to the number of Rhine of the perpendicular image shelf-life VE (= 1200).

[0101] Drawing 20 is the explanatory view showing various kinds of set points at the time of displaying the image memorized by the 2nd image storage section 61 into the 1st image field W01. In this example, zooming of the image memorized by the 2nd image storage section 62 is not carried out, and all of those screens are displayed.

[0102] In addition, although it is possible also about the image of the 1st image storage section 61 to perform zooming of an image and the location of an image field and to make a change of size, in this example, these processings shall not be performed about the image of the 1st image storage section 61. Therefore, the value which shows various kinds of set points over the image of the 1st image storage section 61 to drawing 19 is maintained.

[0103] About the image of the 2nd image storage section 62, while CPU50 computes various kinds of set points according to the following formulas 1, the computed value is set as each circuit.

[Equation 1]

$$Nh = INT(Nh0/Mh)$$

$$fh = fh0/Mh$$

$$Nv = INT(Nv0/Mv)$$

$$fv = fv0/Mv$$

$$Kh1 = \Delta HST$$

$$Kh2 = Lh$$

$$Kv1 = \Delta VST$$

$$Kv2 = Lv$$

Here, a operator "INT" shows the operation which omits the fraction part of the result of an operation in a parenthesis, and takes integer part. moreover, Mh The horizontal scale factor of an image, and Mv Zero O1 which the scale factor of the perpendicular direction of an image, **HST, and **VST have in the upper left of the effective image field of the basic image field W01 from — endpoint O2 at the upper left of the 2nd image field W02 up to — offset of a horizontal direction and a perpendicular direction, and Lh Lv The width of face of the horizontal direction and perpendicular direction of the 2nd image field W02 is shown, respectively.

[0104] When there is no zooming of an image about the image of the 2nd image storage section 62, they are a scale factor Mh and Mv. The set point Nh in the H-PLL section 141 of the 2nd storage control section 72 since both values are 1 The set point Nv in the V-PLL section 142 It is equal to these set points in the 1st storage control section 71. In the example of drawing 20 , since all of the screens of the 2nd image field W02 are displayed, the set point Kh2 of the level viewing-area period counter 135 in the 2nd enabling-signal generation circuit 132 and the set point Kv2 of the perpendicular viewing-area period counter 138 are set as 640 pixels which shows the maximum field of the 2nd image field W02, and 400 lines, respectively.

[0105] Drawing 21 is the explanatory view showing various kinds of set points in the case of displaying a part of the screen, without carrying out zooming of the image of the 2nd image storage section 62. Width of face Lh with the screen horizontal when displaying some screens Vertical width of face Lv Other set points which it is set as a counter 135,138, respectively and are shown in drawing 21 (B) are still standard values. In addition, in the example of drawing 21 , the starting point address AHAL is further set as (640x5+10). 640 is the number of pixels for the 1 scanning line, and is equivalent to the addition address BHBL shown in drawing 16 (A). Therefore, the starting point address AH AL in drawing 21 The value shows that the address reference point Pi (drawing 16 (A)) is set as 5th line the 10th pixel. The address origin/datum Pi is an origin/datum at the time of reading image data from image memory. Therefore, it is possible by changing the value of the starting point address AHAL to read the image data memorized to the field of the arbitration in image memory.

[0106] Drawing 22 is the explanatory view showing various kinds of set points in the case of expanding the image of the 2nd image storage section 62 horizontally, and displaying all of the screens. In this case, the set point Nh of the H-PLL section 141 of the storage control section 72 It is the level scale factor Mh about that certified value Nh0. It is set as the broken value. Moreover, the set point Kh2 of the level viewing-area period counter 135 of the enabling-signal generation circuit 132 is set as the value (= 960) which multiplied the certified value (= 640) by the level scale factor Mh (960/640).

[0107] In addition, level scale factor Mh A value can be inputted using a keyboard. Or it responds to actuation in which an operator changes the size of the 2nd image field W02 using a mouse, and CPU50 is the level scale factor Mh. You may compute. In the case of the latter, it is the horizontal width of face Lh of the 2nd image field W02. It is the level scale factor Mh by breaking by standard width of face (it being 640 pixels about the 2nd image). It asks.

[0108] Horizontal scale factor Mh Frequency fh of the horizontal clock signal CLK2 of modification, then the 2nd storage control section 72 It changes. Since it is equivalent to 1 pixel of the 2nd image field W02, one pulse of a clock signal CLK2 is the level scale factor Mh. Modification changes the period of the clock signal CLK2 equivalent to 1 pixel. As shown in drawing 15 , this clock signal CLK2 is used as a synchronous clock of read-out of the video signal from the image storage section 61, and is used also as synchronizing clock signal DACLK of the D-A conversion section 86. That is, since the frequency of a clock signal CLK2 also changes according to the frequency of the video signal read from the image storage section 62 when an image is expanded horizontally, an image can be expressed as good image quality by carrying out D-A conversion of the video signal synchronizing with this clock signal CLK2.

[0109] in addition, level scale factor Mh ****** — by setting up one or less value, it is also possible to reduce an image horizontally. It is related horizontally and is same in the actuation at the time of expansion, and the actuation at the time of contraction.

[0110] Drawing 23 is the explanatory view showing various kinds of set points in case the image in the 2nd image field W02 is expanded perpendicularly and all of the screens are displayed. The set point Nv of the V-PLL section 142 of the 2nd storage control section 72 It is set as the value which broke the certified value Nv0 by the perpendicular scale factor Mv (= 600/400). Moreover, the set point Kv2 of the perpendicular viewing-area period counter 138 of the 2nd enabling-signal generation circuit 132 is the perpendicular scale factor Mv to the certified value (= 400). It is set as the value (= 600) by which it multiplied. In addition, perpendicular scale factor Mv Level scale factor Mh mentioned above It is set up by the setting approach and the same approach. When an image is expanded perpendicularly, according to the timing chart of above-mentioned drawing 17 , the serial read-out control section 161 performs expansion actuation.
[0111] Drawing 24 is the explanatory view showing various kinds of set points in case the image of the 2nd image field W02 is reduced perpendicularly and all of the screens are displayed. It is the set point Nv of the V-PLL section 142 like [in vertical contraction] the case of expansion. It is set as the value which broke the certified value Nv0 by the perpendicular scale factor Mv (= 286/400). Moreover, the set point Kv2 of the perpendicular viewing-area period counter 138 is the perpendicular scale factor Mv to the certified value (= 400). It is set as the value (= 286) by which it multiplied. When an image is reduced perpendicularly, according to the timing chart of above-mentioned drawing 18 , the serial read-out control section 161 performs contraction actuation.
[0112] As explained above, zooming of an image is realized by work of the H-PLL section 141, the V-PLL section 142 (drawing 8), and the serial read-out control section 161 (drawing 14), and modification of the location of an image field or size is realized by work of the enabling-signal generation circuits 131-133 (drawing 5).
[0113] In addition, although processing of zooming of the image about the image of the 2nd image storage section 62 and processing of modification of the size of the 2nd image field W02 were explained above, it is possible to perform processing with the same said of the image of other two image storage sections 61 and 63. Moreover, level scale factor Mh of an image Perpendicular scale factor MV of an image Offset **HST of an image field, **VST, the size Lh of an image field and LV (namely, Kh2, Kv2), and the starting point address AHAL can be set up independently, respectively.
[0114] E. The configuration and actuation of the animation write control section : drawing 25 is the block diagram showing the internal configuration of the animation write control section 74. The signal and component of the animation write control section 74 are equivalent to the component of the storage control section 71 shown in some the components and drawing 8 of the image control signal generating section 80 shown in drawing 5 , as shown below.
[0115] The correspondence relation of the component of drawing 25 and drawing 5 is as follows.
DRH-PLL section 200: DPLL section 100 perpendicular image starting position counter 201: counter 211:level back-porch period counter 112 level image field period Counter 212: perpendicular back porch period counter 122 perpendicular image field period counter 202: — perpendicular — an image shelf-life counter 123 AND-gate 203:AND-gate 126 level image starting position — Level image shelf-life counter 113AND-gate213: AND-gate 116 perpendicular write-in initiation counter 222: Perpendicular display initiation period counter 137 perpendicular write-in field counter 223: perpendicular viewing-area period counter 138AND-gate224: — an AND-gate 139 level write-in initiation counter 232:level display initiation period — counter 134 level write-in field counter 233:level viewing-area period counter 135AND-gate224: — the AND gate 136 [0116] The correspondence relation of the component of drawing 25 and drawing 8 is as follows.
DV-PLL Section 221: 145 NAND-gate 244:NAND-gate [the V-PLL section 142 DH-PLL section 231:H-PLL section 141 waveform-shaping section 241 the 243:waveform-shaping section 143 -] 146 inverter 251: Inverter 147 [0117] The control clock change-over section 250 of drawing 25 is the circuit which is not in the circuit of drawing 5 and drawing 8 . Moreover, although the animation write control section 74 has the same circuit as the address-generation circuit 148 shown in drawing 8 , illustration is expedient-

upper-omitted in drawing 25 .
[0118] The animation write control section 74 controls the display period of an image synchronizing with Vertical Synchronizing signal DVSYNC and Horizontal Synchronizing signal DHSYNC which are given from video-signal separation / digitization control section 76 (drawing 1). Drawing 26 and drawing 27 are ********** timing charts about actuation of the horizontal direction of the animation write control section 74, and a perpendicular direction. Since drawing 26 and drawing 27 support drawing 6 and drawing 7 which were mentioned above, respectively, they omit the explanation here.
[0119] The control clock change-over section 250 chooses 1st clock signal DRCLK which the DRH-PLL section 200 generates, when the level of the write enable signal WE0 (this corresponds to the lead enable signal RE in drawing 8) is 1 (write inhibit), and when the level of the write enable signal WE0 is 0 (write permission), it chooses 2nd clock signal DDCLK which the DH-PLL section 231 generates. One pulse of 1st clock signal DRCLK supports 1 pixel of the 1st fundamental image field W01. Moreover, one pulse of 2nd clock signal DDCLK is a signal which synchronizes with the video signal which supports 1 pixel at the time of carrying out zooming of the image horizontally, and is written in the image storage section 63. That is, the control clock change-over section 250 supplies 2nd clock signal DDCLK which synchronized with the video signal written in to the 3rd image storage section 63, when writing a video signal in the image storage section 63, and on the other hand, when not writing in a video signal, it supplies 1st clock signal DRCLK which synchronized with the fundamental image to the 3rd image storage section 63.
[0120] The animation write control section 74 generated various kinds of signals VCLW0, HCLW0, INC0, WEO, and CKL0 used for the writing of a video signal to the image storage section 63, and has given them to the image storage section 63. Since these signals correspond to the signals VCLR and HCLR in drawing 8 , and INC, RE and CLK, respectively, they omit explanation.
[0121] F. — the configuration of 3 port image storage section, and : of operation — drawing 28 is the block diagram showing the internal configuration of 3 port image storage section 63. 3 port image storage section 63 has the serial write control section 260, the random read-out / write control section 261, the serial read-out control section 262, and 3 port memory 263. Random read-out / write control section 261 has the same configuration as random read-out / write control section 160 shown in drawing 12 , and has the configuration as the serial read-out control section 161 with the same serial read-out control section 262.
[0122] Drawing 29 is the block diagram showing the internal configuration of 3 port memory 263. 3 port memory 263 is equipped with the memory cell array 165, two selectors 272,273, AND gates 274, and two 3 State buffer sections 275,276. It has the same function as the selector 166 shown in drawing 13 , and, as for the 1st selector 272, two 3 State buffers 275,276 also have the same function as 3 State buffer 167,168 of drawing 13 .
[0123] According to the random write-in signal RWR, the 2nd selector 273 chooses one side of the random data RDATA and serial data RGBI0, and supplies it to the memory cell array 271. The AND gate 274 enables the writing of the memory cell array 271, when at least one side of the serial data write-permission signal SWE0 given from the serial write control section 260 and the random write-in signal RWR given from random read-out / write control section 261 is L level.
[0124] Drawing 30 is the block diagram showing the internal configuration of the serial write control section 260. The components 281-284 of the serial write control section 260, and 286, 290, 292, 294, 296, 298, 300 and 302,304,306,308 are the same as each components 171-174 of the serial read-out control section 161 shown in drawing 14 , and 176, 1800, 182, 184, 186, 188, 190 and 192,194,196,198 respectively. In the serial read-out control section 161, in the serial write control section 260, the reversal output of D flip-flop 309 is given to the AND gate 308 to the output of D flip-flop 199 being outputted as a serial data read-out enabling signal SRD as it is, and the difference between the serial read-out control section 161 and the serial write control section 260 is only the point that the output of the AND gate 308 is outputted as a write-permission signal SWE0.

[0125] Drawing 31 is a timing chart which shows actuation of the serial write control section 260. Since this actuation is almost the same as the actuation of the serial read-out control section 161 shown in drawing 15 , explanation is omitted. It can write image data in the memory area of the arbitration of 3 port memory 263, the serial write control section 260 performing contraction of the perpendicular direction of an image, and horizontal zooming.

[0126] G. modification: — the range which this invention is not restricted to the above-mentioned example, and does not deviate from that summary in addition — setting — various voice — it is possible to set like and to carry out, for example, the following deformation is also possible.

[0127] (1) Instead of using a selector (multiplexer) as the video-signal change-over section 82 shown in drawing 1 , as shown in drawing 32 , video-signal change-over section 82a may be constituted using three 3 State buffers. In this case, what is necessary is to make only one of the three 3 State buffers into enabling state using the signal DMPX which decoded the multiplexer signal MPX.

[0128] (2) Instead of the V-PLL section 142 shown in drawing 8 , as shown in drawing 33 , the PLL circuit 148 and a counting-down circuit 149 may be used. It is the set point Nv of the V-PLL section 142 which the horizontal read-out enabling signal HPIE is inputted into the PLL circuit 148, and shows the set point N to drawing 8 . It is equal to the value which multiplied by 1/of rates M of dividing of a counting-down circuit 149. Here, M is the total number of Rhine of one screen. Since the frequency is higher than the perpendicular read-out enabling signal VPIE inputted into the V-PLL section 142 shown in drawing 8 , the horizontal read-out enabling signal HPIE inputted into the PLL circuit 148 can reduce the jitter of the output signal VCLK.

[0129] (3) Frequency fh in which the clock signal CLK2 outputted from the 2nd storage control section 72 differs from the frequency fh0 of the basic clock signal CLK1 in carrying out zooming of the image read from the 2nd image storage section 62 horizontally, as shown in drawing 22 It has. This is the same also about the clock signal CLK3 outputted from the 3rd image storage section 63. However, if zooming of the image is not carried out horizontally, three clock signals CLK1-CLK3 have the equal frequency mutually. therefore, the video signal read from the 2nd and 3rd image storage section 62 and 63 in the 1st clock signal CLK1 when zooming of the image did not have to be carried out horizontally — use — things are made. In this case, what is necessary is to omit the clock signal change-over section 84 in the circuit of drawing 1 , and just to supply the 1st clock signal CLK1 to the direct D-A conversion section 86.

[0130] (4) In the example of drawing 1 , although the image was displayed on the color monitor 90 according to the analog video signal, the display which can display an image according to a digital video signal can also be used. In this case, what is necessary is to omit the D-A transducer 86 and an amplifier 88 and just to supply directly clock signal DACLK chosen in the digital video signal RGB 0 chosen in the video-signal change-over section 82, and the clock signal change-over section 84 to a digital graphic display device.

[0131] (5) The memory control means in the invention in this application is realized by the combination of the serial read-out control section (drawing 12 , drawing 28) contained in the image storage sections 61-63, respectively, and the three storage control sections 71-73 (drawing 8). In addition, the read-out control section of the image storage sections 61-63 and the write control section may be prepared as a circuit in the memory chip which realizes the image storage sections 61-63, and you may make it prepare them in the same circuit as the storage control sections 71-73.

[0132] (6) The selection-signal output means in the invention in this application is realized by the storage section 60, and the multiplexer signal MPX (drawing 1) is equivalent to the image selection signal in the invention in this application. However, it is also possible to adopt various circuits other than storage section 60 as a means to output the multiplexer signal MPX. For example, it is also possible to adopt the circuit which memorizes the location of each four top-most vertices of three image fields W01-W03 shown in drawing 4 , computes change-over location A-F for every scanning line based on these top-most-vertices locations, and generates the multiplexer signal MPX by this. Moreover,

multiplexer data are memorized in memory as run length data for every scanning line, and it is also possible to generate the multiplexer signal MPX based on this run length data. In these modifications, the amount of memory which multiplexer data take can be reduced.

[0133] (7) Although read-out of the multiplexer signal MPX is performed in the above-mentioned example by supplying various kinds of signals which the storage control section 71 generated also to the storage section 60, you may make it prepare the control section of storage section 60 dedication. However, if the signal which the storage control section 71 generated is also given to the storage section 60 like the above-mentioned example, there is an advantage that the component part of the whole circuit can be reduced.

[0134]

[Effect of the Invention] It is effective in the ability to display two or more images on two or more image memory in piles on one screen according to the image data memorized, respectively, without transmitting image data among two or more image memory according to invention indicated by claim 1, as explained above.

[0135] Moreover, since according to invention indicated by claim 2 the image select data is memorized in memory and this image select data is read as an image selection signal, it is effective in an image selection signal being easily generable.

[0136] According to invention indicated by claim 3, it is effective in the circuit of the dedication for generating a select data read-out control signal becoming unnecessary, and circuitry becoming easy.

[0137] Since the clock signal which was suitable for each video signal, respectively performs D-A conversion according to invention indicated by claim 4, it is effective in the ability to express an image as good image quality.

[0138] According to invention indicated by claim 5, it is effective in the ability to carry out variable power of the image horizontally by changing the value of the integer N1 set as the 1st PLL circuit.

[0139] According to invention indicated by claim 6, a processor is an integer N1. By changing a setup, it is effective in the ability to carry out variable power of the image horizontally.

[0140] According to invention indicated by claim 7, it is effective in the ability to carry out variable power of the image perpendicularly by changing the value of the integer N2 set as the 2nd PLL circuit.

[0141] According to invention indicated by claim 8, a processor is an integer N2. By changing a setup, it is effective in the ability to carry out variable power of the image perpendicularly.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The block diagram showing the configuration of a computer system equipped with the graphic display device as one example of this invention.

[Drawing 2] The explanatory view showing the relation between the room of the storage sections 60-63, and a screen display.

[Drawing 3] The explanatory view showing the address map of OS using the three image storage sections.
[Drawing 4] The explanatory view showing relation with a screen display in the read-out enabling signals VPIE and HPIE and color monitor 90 which are outputted from the image control signal generating section 80.
[Drawing 5] The block diagram showing the internal configuration of the image control signal generating section 80.
[Drawing 6] The horizontal timing chart of the image control signal generating section 80.
[Drawing 7] The timing chart of the perpendicular direction of the image control signal generating section 80.
[Drawing 8] The block diagram showing the internal configuration of the storage control section 71.
[Drawing 9] The timing chart which shows actuation of the storage control section 71.
[Drawing 10] The block diagram showing the configuration of the waveform-shaping sections 143-145.
[Drawing 11] The timing chart which shows actuation of the waveform-shaping section.
[Drawing 12] The block diagram showing the internal configuration of the storage section 61.
[Drawing 13] The block diagram showing the internal configuration of memory 162.
[Drawing 14] The block diagram showing the internal configuration of the serial read-out control section 161.
[Drawing 15] The timing chart which shows actuation of the serial read-out control section 161.
[Drawing 16] The conceptual diagram showing the relation of the screen and the address corresponding to memory.
[Drawing 17] The timing chart which shows actuation of the serial read-out control section 161 at the time of perpendicular direction expansion of an image.
[Drawing 18] The timing chart which shows actuation of the serial read-out control section 161 at the time of perpendicular direction contraction of an image.
[Drawing 19] The explanatory view showing the storage control section 71 at the time of displaying only the 1st image, and various kinds of set points of the enabling-signal generation circuit 131.
[Drawing 20] The explanatory view showing various kinds of set points in case there is no zooming of the 2nd image and all of the screens are displayed.
[Drawing 21] The explanatory view showing various kinds of set points in case there is no zooming of the 2nd image and a part of the screen is displayed.
[Drawing 22] The explanatory view showing various kinds of set points in case the 2nd image is expanded horizontally and all of the screens are displayed.
[Drawing 23] The explanatory view showing various kinds of set points in case the 2nd image is expanded perpendicularly and all of the screens are displayed.
[Drawing 24] The explanatory view showing various kinds of set points in case the 2nd image is reduced perpendicularly and all of the screens are displayed.
[Drawing 25] The block diagram showing the internal configuration of the animation write control section 74.
[Drawing 26] The timing chart which shows horizontal actuation of the animation write control section 74.
[Drawing 27] The timing chart which shows actuation of the perpendicular direction of the animation write control section 74.
[Drawing 28] The block diagram showing the internal configuration of 3 port image storage section 63.
[Drawing 29] The block diagram showing the internal configuration of 3 port memory 263.
[Drawing 30] The block diagram showing the internal configuration of the serial write control section 260.
[Drawing 31] The timing chart which shows actuation of the serial write control section 260.
[Drawing 32] The block diagram showing other configurations of the video-signal change-over section.
[Drawing 33] The block diagram showing other configurations of the V-PLL section.

[Drawing 34] The explanatory view showing the display action in the conventional graphic display device.

[Description of Notations]

40 — Keyboard
42 — Mouse
50 — CPU
52 — CPU bus
60 — Storage section
61–63 — Image storage section
71–73 — Storage control section
74 — Animation write control section
76 — Video-signal separation / digitization control section
78 — Animation data decompression section
80 — Image control signal generating section
82 82a — Video-signal change-over section
84 — Clock signal change-over section
86 — D-A conversion section
88 — Amplifier
90 — Color monitor
100 — The DPLL section
111 — Horizontal synchronization period counter
112 — Level back porch period counter
113 — Level image shelf-life counter
114 — Level front porch period counter
115 — Level reset counter
116 — AND gate
121 — Vertical-synchronization period counter
122 — Perpendicular back porch period counter
123 — Perpendicular image shelf-life counter
124 — Perpendicular front porch period counter
125 — Perpendicular reset counter
126 — AND gate
131–133 — Enabling-signal generation circuit
134 — Level display initiation period counter
135 — Level viewing-area period counter
136 — AND gate
137 — Perpendicular display initiation period counter
138 — Perpendicular viewing-area period counter
139 — AND gate
141 — H-PLL section
142 — V-PLL section
143–145 — Waveform-shaping section
146 — NAND gate
147 — Inverter
148 — Address-generation circuit
151,152 — D flip-flop
153 — AND gate
160 — Random read-out / write control section
161 — Serial read-out control section
162 — Memory

165 — Memory cell array
166 — Selector
167,168 — 3 State buffer
171–174 — Address register
176 — Decoder
180,182,184 — Adder
186,188 — Latch
190 — Level counter
192,194,196,198 — AND gate
199 — D flip–flop
200 — DRH–PLL section
201 — Perpendicular image starting position counter
202 — Perpendicular image field period counter
203 — AND gate
211 — Level image starting position counter
212 — Level image field period counter
213 — AND gate
221 — DV–PLL section
222 — Perpendicular write–in initiation counter
223 — Perpendicular write–in field counter
224 — AND gate
231 — DH–PLL section
232 — Level write–in initiation counter
233 — Level write–in field counter
241–243 — Waveform–shaping section
244 — NAND gate
250 — Control clock change–over section
260 — Serial write control section
261 — Random read–out / write control section
262 — Serial read–out control section
271 — Memory cell array
272,273 — Selector
274 — AND gate
275,276 — 3 State buffer
320 — PLL circuit
321 — Counting–down circuit
AHAL — Starting point address
ADBUS — Address bus
ADSEL — Address selection signal
AEN — Address valid signal
AR, AG, AB — Analog video signal
BHBL — Addition address
CLK1–CLK3 — Clock signal
DACLK — Clock signal
DDCLK — Clock signal
DHSYNC — Horizontal Synchronizing signal
DRCLK — Clock signal
DTCLK — Dot clock signal
DVSYNC — Vertical Synchronizing signal

HB — Level back porch period
HCLR — Level reset signal
HE — Level image shelf-life
HF — Level front porch period
HPIE, HPIE1-HPIE3 — Perpendicular read-out enabling signal
HR — Level reset period
HS — Horizontal synchronization period
HSYNC — Horizontal Synchronizing signal
HYENB — Horizontal effective enable signal
INC — Perpendicular increment signal
Mh — Level scale factor
Mv — Perpendicular scale factor
MPX — Multiplexer signal
Pi — Address reference point
RADDRS — Random address
RDATA — Random data
RE — Lead enable signal
RGB 01-03, RGBI0 — Video signal
RRD — Random read-out signal
RWR — Random write-in signal
SADDRS — Serial address
SRD — Serial read-out enabling signal
SWE0 — Write-permission signal
VB — Perpendicular back porch period
VCLK — Clock signal
VCLR — Perpendicular reset signal
VE — Perpendicular image shelf-life
VF — Perpendicular front porch period
VPIE, VPIE1-VPIE3 — Horizontal read-out enabling signal
VR — Perpendicular reset period
VS — Vertical-synchronization period
VSYNC — Vertical Synchronizing signal
VYENB — Perpendicular effective enable signal
W01-W03 — Image field
WE0 — Write enable signal

[Translation done.]